REMARKS

Claims 1-16 are pending in this application, of which Applicants propose to amend claims 1, 3, 5, 8, 9, 12, 13, 15, and 16.

Claim Amendments

Applicants propose to amend claims 1, 3, 5, 8, 9, 12, 13, 15, and 16 to further clarify the claim language. These amendments are supported at page 9, lines 31-33 of the Specification of the instant application. Furthermore, these amendments are not made for reasons related to patentability.

§112, Second Paragraph, Rejection of Claims 1-16

The Examiner rejected claims 1-16 under 35 U.S.C. § 112, second paragraph, because the term "test vectors that pass through the changed logic cones" in claims 1, 3, 5, 8, 9, 12, 13, 15, and 16 is allegedly vague and indefinite. Claims 1, 3, 5, 8, 9, 12, 13, 15, and 16 are proposed to be amended to recite "test vectors that activate the changed logic cones." Thus, claims 1, 3, 5, 8, 9, 12, 13, 15, and 16, and claims 2, 4, 6, 7, 10, 11, and 14 that depend therefrom, should be allowed over § 112, second paragraph.

§102(b) Rejection of Claims 1-16 over Gilbert et al.

The Examiner rejected claims 1-16 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,805,861 to Gilbert et al. ("*Gilbert et al.*"). Applicants respectfully traverse the rejection for the following reasons.

In order to properly anticipate Applicants' claimed invention under 35 U.S.C. § 102, each and every element of the claim at issue must be found in the reference, either

expressly described or under principles of inherency. Furthermore, "the elements must be arranged as required by the claim." M.P.E.P. § 2131. See also *Richardson v. Suzuki Motor Co., Ltd.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913 (Fed. Cir. 1989).

Claim 1

Gilbert et al. fails to anticipate claim 1 for at least the reason that *Gilbert et al.* does not disclose a circuit designing apparatus comprising, inter alia, "**a logic verification unit configured to perform a logic verification by inputting a plurality of test vectors necessary for the logic verification to a circuit description** ..." and "**a test vector classifying unit configured to classify the test vectors into test vectors that activate the changed logic cones and test vectors that do not activate the changed logic cones using the profile information**," as recited in claim 1.

Instead, *Gilbert et al.* discloses "[a] method used by an electronic design automation system for stabilizing the names of components and nets of an integrated circuit from one design version to another" (Abstract). A Cone Graph Compare (CGC) module reads an old design and a new design from a Logic Design Database. "The CGC module then corrects the component and net names ... by analyzing the cones of logic contained in the design, comparing the old and new designs and assigning new names as needed. ... [T]he CGC module writes the name corrected design into the Logic Design Database" (Col. 11, line 62 to Col. 12, line 9).

In reference to claim 1, the Examiner alleges that the "user-defined names" (disclosed at Col. 11, lines 55-61) and "new names" (disclosed at Col. 12, line 28) of

Gilbert et al. constitute the "test vectors" (Office Action, pp. 3-4). A test vector is an assignment of values to input variables of the circuit description to simulate the circuit that is described by the circuit description. One of ordinary skill in the art would not consider a "name" to constitute this "test vector." Thus, the "user-defined names" and "new names" of *Gilbert et al.* do not constitute "test vectors" as recited in claim 1.

Moreover, *Gilbert et al.* does not disclose the "logic verification unit" and the "test vector classifying unit" for at least the reason that *Gilbert et al.* does not disclose the "plurality of test vectors," arranged as required by claim 1. Even if a "name" could constitute a "test vector," the Examiner, in reference to the "test vector classifying unit" recited in claim 1, apparently relies on the different "new names" of *Gilbert et al.* to constitute a "test vector" (Office Action, pg. 4). The "user-defined names" and the "new names" of *Gilbert et al.* are not arranged as required by claim 1 because the "user-defined names" and the "new names" are not the same names. The "[n]ew component and net names are generated for the new logic design ..." (Col. 11, lines 17-18). However, the "user-defined names" are "user-defined." "All user-defined names are retained by CGC processing." (Col. 11, lines 14-15). In contrast to *Gilbert et al.*, claim 1 specifies that the "plurality of test vectors" inputted by the logic verification unit are the same as "the test vectors" classified by the test vector classifying unit of claim 1. Thus, since the "user-defined names" and the "new names" of *Gilbert et al.* are not arranged as required by claim 1, *Gilbert et al.* fails to teach the "logic verification unit" and the "test vector classifying unit" recited in claim 1.

Thus, since *Gilbert et al.* fails to teach the "logic verification unit" and the "test vector classifying unit" recited in claim 1, claim 1 and claims 2 and 12-14 that depend therefrom are allowable over *Gilbert et al.* under § 102(b).

Claim 3

Gilbert et al. also does not anticipate independent claim 3 for at least the reason that *Gilbert et al.* fails to disclose a circuit designing method comprising, inter alia, "**performing a logic verification by inputting a plurality of test vectors necessary for the logic verification to a circuit description defining a structure and a specification of a circuit to be designed and comparing an output signal and an expected value of the output signal, and judging the validity of the circuit description**" and "**classifying the test vectors into test vectors that activate the changed logic cones and test vectors that do not activate the changed logic cones, based on the profile information**," as recited in amended claim 3.

As explained above, neither the "user-defined names" nor the "new names" of *Gilbert et al.* constitute "test vectors" that are inputted to a circuit description in performing a logic verification and "activate logic cones," as required by claim 3. Rather, the "user-defined names" and the "new names" of *Gilbert et al.* are "names". A "name" does not constitute a test vector, which is an assignment of values to input variables of the circuit description to simulate the circuit that is described by the circuit description. For example, *Gilbert et al.* does not teach that these "names" can be inputted to a circuit description to perform a logic verification, or that these "names" can activate logic cones.

Moreover, *Gilbert et al.* does not disclose the "plurality of test vectors," arranged as required by claim 3. In reference to "performing a logic verification," recited in claim 3, the Examiner alleges that the "user-defined names" disclosed at Col. 11, lines 55-61, of *Gilbert et al.*, constitute the "test vectors" (Office Action, pg. 3). However, in reference to "classifying the test vectors," recited in claim 3, the Examiner relies on the "new names" disclosed at Col. 12, lines 28-30, of *Gilbert et al.* (Office Action, pg. 3). The "user-defined names" and the "new names" of *Gilbert et al.* are not the same names, in contrast to the "plurality of test vectors" inputted in performing the logic verification of claim 3 and "the test vectors" classified in classifying the test vectors of claim 3, which are the same test vectors.

Thus, since *Gilbert et al.* fails to teach "performing a logic verification" and "classifying the test vectors" as recited in claim 3, claim 3 and claims 4-7 and 15 that depend therefrom are allowable over *Gilbert et al.* under § 102(b).

Claim 8

Additionally, *Gilbert et al.* fails to anticipate independent claim 8 for at least the reason that *Gilbert et al.* does not disclose a computer-readable recording medium storing a circuit designing program comprising and making a computer execute, inter alia, "**instructions configured to perform a logic verification by inputting a plurality of test vectors necessary for the logic verification into a circuit description defining a structure and a specification of a circuit to be designed and comparing an output signal and an expected value of the output signal, and judging the validity of the circuit description**" and "**instructions configured to classify the test vectors into test vectors that activate the changed logic cones and test vectors**

that do not activate the changed logic cones, based on the profile information," as recited in amended claim 8.

As explained above, neither the "user-defined names" nor the "new names" of *Gilbert et al.* constitute "test vectors" that are inputted to a circuit description in performing a logic verification and "activate logic cones," as required by claim 8. The "user-defined names" and the "new names" of *Gilbert et al.* are "names," and a "name" does not constitute a test vector, which is an assignment of values to input variables of the circuit description to simulate the circuit that is described by the circuit description. For example, *Gilbert et al.* does not teach that these "names" can be inputted to a circuit description to perform a logic verification, or that these "names" can activate logic cones.

Moreover, *Gilbert et al.* does not disclose the "plurality of test vectors," arranged as required by claim 8. In reference to the "instructions configured to perform a logic verification" recited in claim 8, the Examiner alleges that the "user-defined names" disclosed at Col. 11, lines 55-61, of *Gilbert et al.*, constitute the "test vectors" (Office Action, pg. 2). However, in reference to the "instructions configured to classify the test vectors" recited in claim 8, the Examiner relies on the "new names" disclosed at Col. 12, lines 28-30, of *Gilbert et al.* (Office Action, pg. 3). The "user-defined names" and the "new names" of *Gilbert et al.* are not the same names, in contrast to the "plurality of test vectors" inputted by the instructions configured to perform a logic verification of claim 8 and "the test vectors" classified by the instructions configured to classify the test vectors of claim 8, which are the same test vectors.

Thus, since *Gilbert et al.* fails to teach the "instructions configured to perform a logic verification" and the "instructions configured to classify the test vectors" recited in claim 8, claim 8 and claims 9-11 and 16 that depend therefrom are allowable over *Gilbert et al.* under § 102(b).

CONCLUSION

Applicants respectfully requests that this Amendment under 37 C.F.R. § 1.116 be entered by the Examiner, placing claims 1-16 in condition for allowance. Applicants submit that the proposed amendments of claims 1, 3, 5, 8, 9, 12, 13, 15, and 16 do not raise new issues or necessitate the undertaking of any additional search of the art by the Examiner, since all of the elements and their relationships claimed were either earlier claimed or inherent in the claims as examined. Therefore, this Amendment should allow for immediate action by the Examiner.

In view of the foregoing remarks, Applicants submit that this claimed invention, as amended, is neither anticipated nor rendered obvious in view of the prior art references cited against this application. Applicants therefore request the entry of this Amendment, the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our Deposit Account No. 06-0916.

Respectfully submitted,

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